ADM-XRC-KU1
User Manual

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Table Of Contents

List of Tables

List of Figures

1 Introduction

The **ADM-XRC-KU1** is a high-performance XMC for applications using Kintex Ultrascale FPGAs from Xilinx.

The **ADM-XRC-KU1** includes a separate FPGA with a PCIe bridge developed by Alpha Data.

The **ADM-XRC-KU1** is available in air-cooled and conduction-cooled configurations. View the ADM-XRC-KU1 Ordering Info tab at ADM-XRC-KU1 Product Page on www.alpha-data.com.

1.1 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0 and 42.3
- PCI Express® Gen2 x4 through the Bridge FPGA with an optional Gen3 x4 PCI Express® link direct to the target FPGA.
- Gen3 x8 PCI Express® link direct to the target when the Bridge FPGA is in USB mode.
- An optional Gen3 x8 PCI Express® link provided through Pn6 using a compatible XMC carrier.
- Support for Kintex Ultrascale FPGA in FLVA1517 package.
- 4 independent banks of DDR4-2400 SDRAM, 2GB/bank (x32), 8GB total.
- Front-panel (XRM2) interface with adjustable voltage, 146 GPIO signals and 8 GT links to user FPGA.
- Rear-panel (XMC) interface with 38 single ended GPIO signals at 3.3V logic levels & 10 GT links between user FPGA and P6.
- Rear-panel (PMC) interface with 64 GPIO signals between user FPGA and P4 (optional) to be used with signals operating at or below 1.8V only.
- Voltage and temperature monitoring.
- Board management via PCI Express® or via USB.
- Air-cooled and conduction-cooled configurations.

1.2 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.2	*XMC Serial RapidIO Protocol Layer Standard*, Feb 2006, VITA, ISBN 1-885731-41-8
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/VITA 46.9	*PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the ADM-XRC-KU1 Software Development Kit (SDK) installation CD. The ADM-XRC-KU1 SDK contains drivers, examples for host control and FPGA design and comprehensive help on application interfacing.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Motherboard / Carrier Requirements

The **ADM-XRC-KU1** is a single width XMC.3 mezzanine with optional P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

The Secondary XMC connector, P6 has a pinout compatible with various XMC to VPX signal maps as defined by VITA 46.9. Please consult the pinouts in this user-guide as-well as those of the carrier manufacturer prior to installation. Assistance can be provided by Alpa Data.

IMPORTANT
Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The **ADM-XRC-KU1** is compatible with either 5V or 12V on the "VPWR" power rail.

2.2.2.1 Installation in ADC-EMC-II Carrier

The Alpha Data ADC-EMC-II carrier accepts both PMC and XMC mezzanine cards. By default, the carrier is configured for PMCs and connects all the serial links from the XMC connector J15 to J25.

To configure for XMC and enable the PCIe interfaces at J15 and J25, switches 1-3 and 1-4 must be ON (closed).

2.2.3 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section 3.7 for further details.

3 Functional Description

3.1 Overview

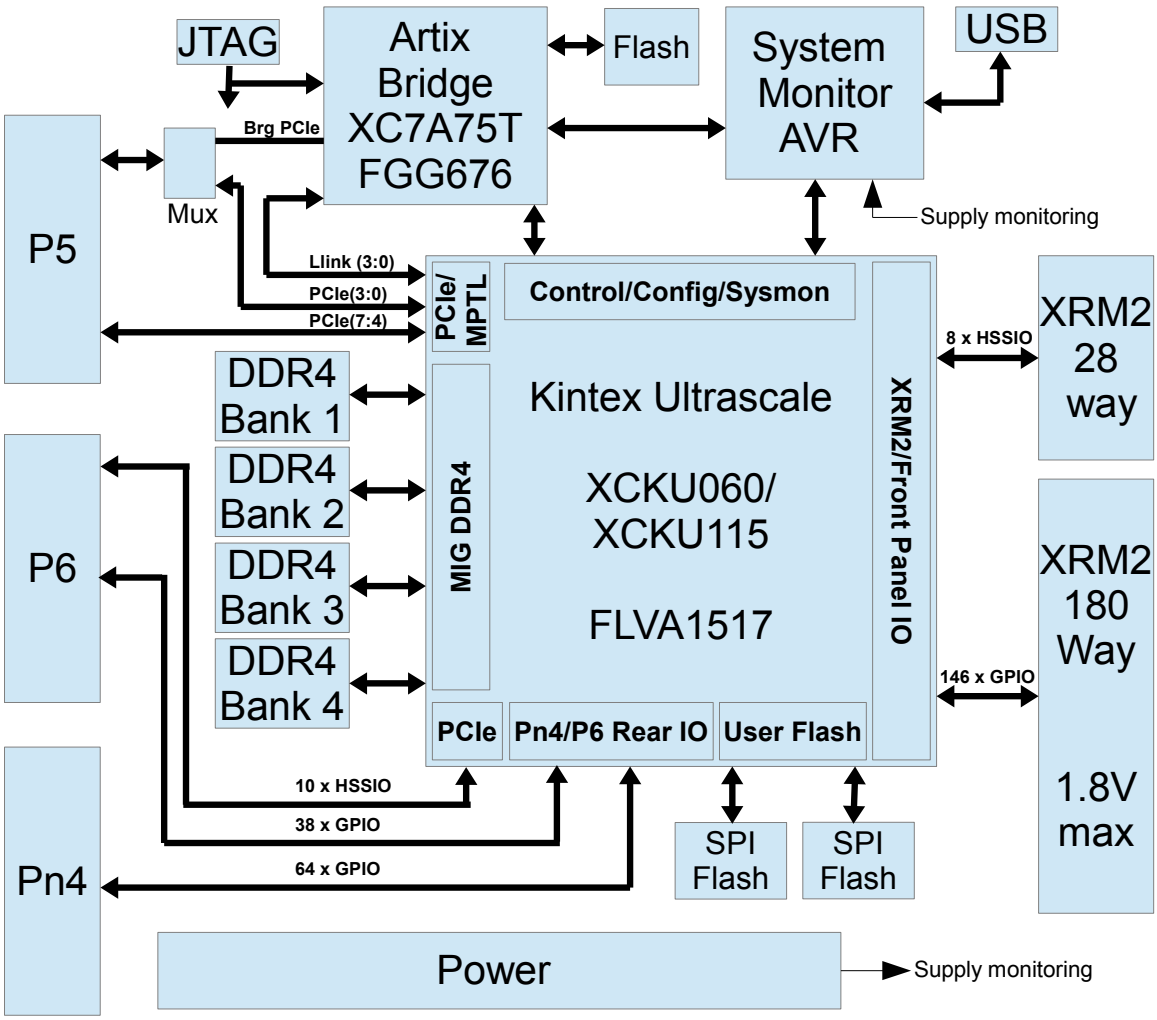


Figure 1 : ADM-XRC-KU1 Block Diagram

3.1.1 Switch Definitions

There is a set of eight DIP switches placed on the rear of the board. Their functions are described in Switch Definitions.

Note:
All switches are OFF by default. *Factory Configuration* switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	Reserved	-	Normal Operation
SW1-2	Reserved	-	Normal Operation
SW1-3	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA.	Bridge FPGA is used. PCIe lanes (3:0) are connected to the bridge.
SW1-4	Flash Boot Inhibit	Target FPGA is not configured from onboard flash memory.	Target FPGA is configured from on-board flash memory.
SW1-5	XMC JTAG	Connect JTAG chain to P5	Isolate JTAG chain from P5
SW1-6	Reserved	-	Normal Operation
SW1-7	*Factory Configuration*	-	Normal Operation
SW1-8	Reserved	-	Normal Operation

Table 2 : Switch Definitions

3.1.2 LED Definitions

The position and description of the board status LEDs are shown in LED Locations:

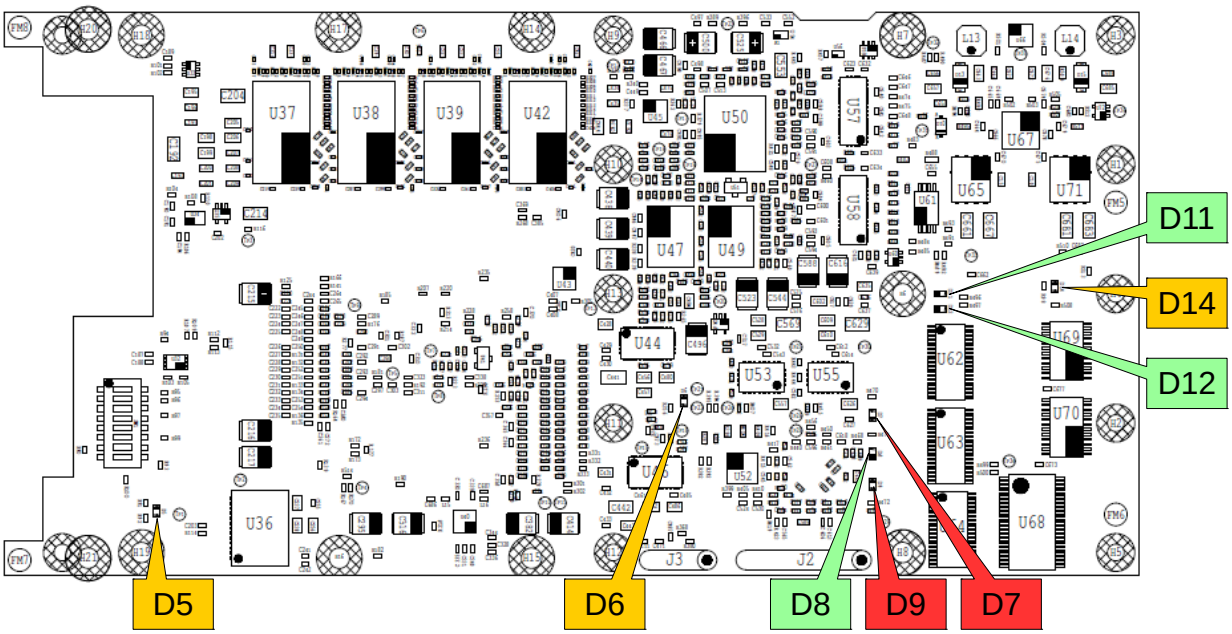


Figure 2 : LED Locations

Comp. Ref.	Function	ON State	Off State
D5(Amber) [1]	Bridge Bypass	Bridge FPGA is bypassed - PCIe lanes (3:0) are connected directly to the user FPGA	Bridge FPGA is used. PCIe lanes (3:0) are connected to the Bridge FPGA.
D6(Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories
D7(Red)	Power Fault	Power supply fault	Normal operation
D8(Green)	Status 0	See Status LED Definitions	
D9(Red)	Status 1	See Status LED Definitions	
D11(Green)	Target Done	Target FPGA is configured	Target FPGA is unconfigured
D12(Green)	Bridge Done	Bridge FPGA is configured	Bridge FPGA is unconfigured
D14(Amber)	XMC JTAG	On-board JTAG chain connected to P5	On-board JTAG chain is isolated from P5

Notes:
1 - The polarity of this LED was reversed on revision 1 boards. This error was corrected on revision 2 onwards.

Table 3 : LED Definitions

3.2 XMC Platform Interface

3.2.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

3.2.2 MBIST#

Built-In Self Test. This output signal is driven active (low) until the FPGA with PCIe interface is configured. In normal operation, this is the Bridge FPGA. In Bridge Bypass mode, it is the target FPGA.

3.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D6.

The MVMRO signal has a 100KΩ pull-down resistor fitted by default. A pull-up can be fitted instead as a manufacturing option - please contact Alpha Data for further details.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the Bridge FPGA at pin M6.

3.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. When asserted, the Bridge FPGA will be reset.

The MRSTI# signal is also passed through the Bridge FPGA and connected to the Target FPGA at pin AE15.

3.2.5 MRSTO#

XMC Reset Out. This optional output signal is driven from the Target FPGA pin J3.

3.2.6 MPRESENT#

Module Present. This output signal is connected directly to 0V.

3.3 JTAG Interface

3.3.1 On-board Interface

A JTAG boundary scan chain is connected to header J2. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The JTAG Header pinout is shown in JTAG Header J2:

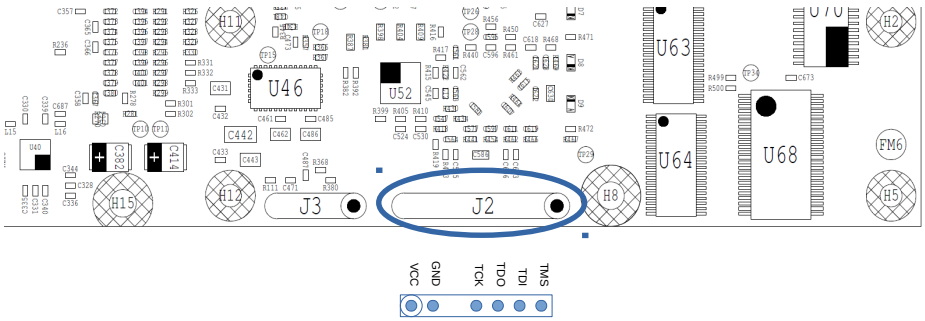


Figure 3 : JTAG Header J2

The scan chain is shown in JTAG Boundary Scan Chain:

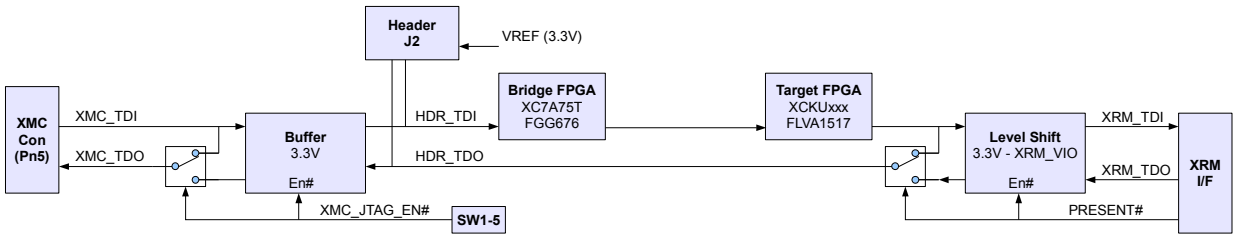


Figure 4 : JTAG Boundary Scan Chain

The clock line on this JTAG interface (HDR_TCK) has a parallel termination (49.9Ω + 22pF to ground) located underneath the XRM Connector (CN1).

If the boundary scan chain is connected to the interface at the XMC connector (SW1-5 is ON), Header J1 should not be used.

3.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The clock line on this JTAG interface (XMC_TCK) has a parallel termination (49.9Ω + 22pF to ground) located underneath the 3.3V buffer (U1).

The interface can be connected to the on-board interface (through level-translators) by switching SW1-5 ON. See Switch Definitions

3.3.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on J2 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 375mA.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

The JTAG signals at the XRM interface use the adjustable voltage XRM_VIO.

3.4 Clocks

The **ADM-XRC-KU1** provides a wide variety of clocking options. On top of fixed 250MHz and 300MHz oscillators and clocks routed from the rear and front panel connectors, the board has 2 user-programmable clock generators. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-XRC-KU1** is given in Clocks. A description of each clock follows.

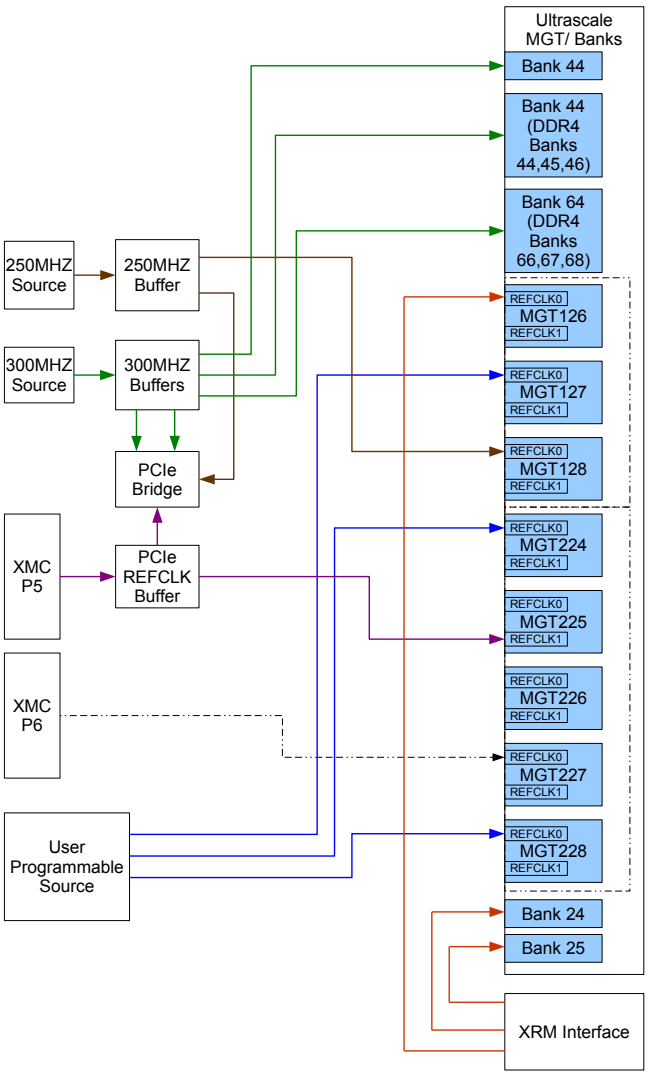


Figure 5 : Clocks

3.4.1 300MHz Reference Clocks (REFCLK300M and FABRIC_CLK)

The fixed 300MHz reference clocks REFCLK300M and FABRIC_CLK are differential LVDS signals.

REFCLK300M is used as the input clock for both DDR4 SDRAM interfaces.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK300M	300 MHz	IO_L14_T2L_GC_44	LVDS	AK22	AL22
REFCLK300M	300 MHz	IO_L11_T1U_GC_64	LVDS	AN18	AN17
FABRIC_CLK	300 MHz	IO_L12_T1U_GC_44	LVDS	AM21	AN21

Table 4 : REFCLK200M Connections

3.4.2 250MHz Reference Clock (REFCLK250M)

The fixed 250MHz reference clocks REFCLK250M is a differential LVDS signal.

REFCLK300M is used as the input clock for the MPTL interface.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK250M	250 MHz	MGTREFCLK0_128	LVDS	T32	T33

Table 5 : REFCLK250M Connections

3.4.3 PCIe Reference Clock 0 (PCIEREFCLK0)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This clock is buffered into two PCIe Express reference clocks that are forwarded to the Bridge and User FPGA respectively.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK	100 MHz	MGTREFCLK0_225	LVDS	AK10	AK9

Table 6 : PCIEREFCLK Connections

3.4.4 PCIe Reference Clock 1 (PCIEREFCLK1)

The reference clock "PCIEREFCLK1" is a differential clock provided by a carrier card through the Secondary XMC connector P6 at pins A19 and B19. The Default build configuration for this board connects this pair to an MGT clock input. Most needed reference clocks can be generated through the User Programmable clocking options. If it is a requirement that this differential pair be utilized as a signal to an MGT bank, a resistor fit option is available. Please contact Alpha Data for details.

3.4.5 Programmable Clocks (LCLK, PROGCLK 0-2)

There are two programable clock sources that are forwarded throughout the FPGA. These clocks are programmable through the Alpha Data ADM-XRC-KU1 SDK. LCLK is generated in the Bridge FPGA by the the Alpha Data ADB3 driver and offers a less accurate frequency resolution, but with a wider programmable frequency range. PROGCLK[2:0] is generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments). PROGCLK[2:0] are all buffered copies of the same clock signal.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
LCLK	5 - 700 MHz	IO_L12_T1U_GC_64	LVDS	AM19	AN19
PROGCLK0	5 - 312.5 MHz	MGTREFCLK1_127	LVDS	Y32	Y33
PROGCLK1	5 - 312.5 MHz	MGTREFCLK1_228	LVDS	AA8	AA7
PROGCLK2	5 - 312.5 MHz	MGTREFCLK1_224	LVDS	AT10	AT9

Table 7 : PROGCLK Connections

3.4.6 Module-Carrier Global Clock (GCLK_M2C)

The clock "GCLK_M2C" is a differential clock signal using LVDS. It is provided by an XRM module through the XRM connector, CN1, at pins 110 & 108. It is connected to an MRCC input on the Target FPGA.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
GCLK_M2C	Variable	IO_L12_T1U_GC_25	LVDS	AR38	AT38

Table 8 : GCLK_M2C Connections

3.4.7 Module-Carrier MGT Clock (MGTCLK_M2C)

The reference clock "MGTCLK_M2C" is a differential clock signal using LVDS. The clock is provided by an XRM module through the XRM connector, CN1, at pins 109 & 111. It is connected to GTH Quad 126 on the Target FPGA for application specific frequencies / line rates.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
MGTCLK_M2C	Variable	MGTREFCLK0_126	LVDS	AD32	AD33

Table 9 : MGTCLK_M2C Connections

3.4.8 Carrier-Module Clock (XRM_PECL)

The clock "XRM_PECL" is a differential clock signal using LVDS levels. The clock is provided by the target FPGA and connected to an XRM module through the XRM connector, CN1, at pins 113 & 115.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
XRM_PECL	Variable	IO_L12_T1U_GC_24	LVDS	AM31	AN31

Table 10 : XRM_PECL Connections

3.5 Flash Memory

A 1Gb Flash Memory (Intel / Numonyx PC28F00AP30EF) is used to store configuration bitstreams for the Bridge and Target FPGAs.

The flash memory cannot be accessed by the target FPGA. Host access is only possible through the FLCTL, FLPAGE and FLDATA registers in the Bridge FPGA.

The region of memory between addresses 0x11000000 and 0x11FFFFFF is allocated for custom data to be stored by the **ADM-XRC-KU1** user.

Utilities for erasing, programming and verification of the flash memory are provided in the ADM-XRC-KU1 SDK.

Write Protect

The Flash Write Protect (WP#) pin is connected to an inverted version of the NVMRO signal at the XMC interface. When the NVMRO signal is active (High), all writes to the flash will be inhibited. This state will be indicated by the Amber LED as shown in LED Locations.

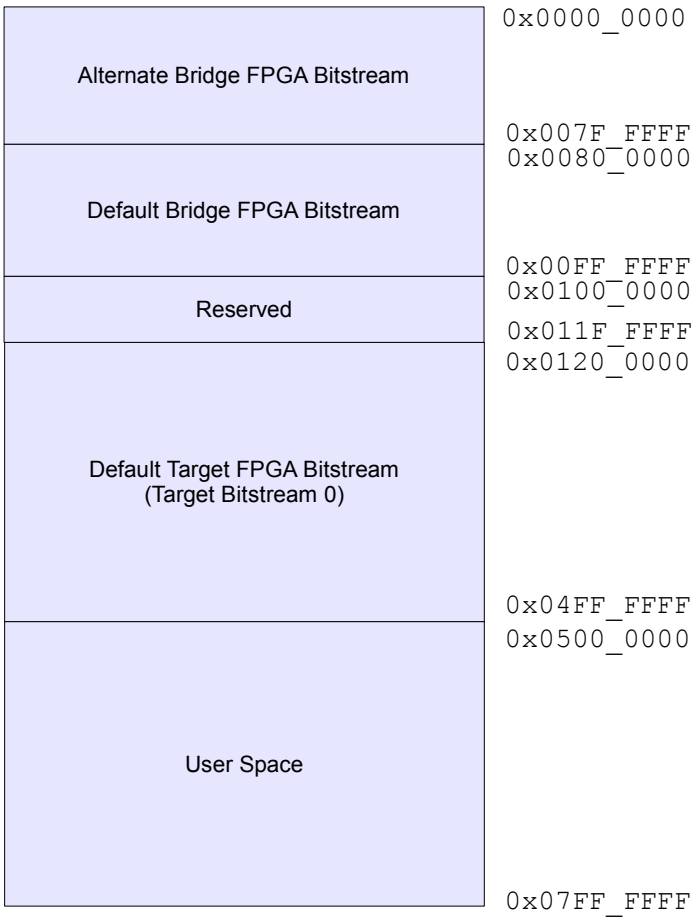


Figure 6 : Flash Memory Map

3.6 Configuration

3.6.1 Power-Up Sequence

If valid data is stored in the flash memory, the Bridge FPGA will automatically configure the Target FPGA at power-up.

This sequence can be inhibited by turning the Flash Boot Inhibit (FBI) switch, SW1-4 to ON. (See Switch Definitions).

> **Note:**
> If an over-temperature alert is detected from the System Monitor, the target **will be cleared** by pulsing its PROG signal. See Automatic Temperature Monitoring.

3.7 Health Monitoring

The **ADM-XRC-KU1** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares the information with blockram in the Bridge FPGA.

The following voltage rails and temperatures are monitored:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12.0V	Board Input Supply
5.0V	Internally generated 5V supply
3.3V	Board Input Supply
2.5V	Level Translation
1.8V	Flash Memory, FPGA IO Voltage (VCCO)
0.95V	Target FPGA Core Supply (VccINT)
1.8V	Target Transceiver Power (AVCC_AUX)
1.2V	DDR4 SDRAM, Target FPGA memory I/O
XRM_VIO	(Front-Panel) I/O voltage
1.0V	Bridge FPGA Core Supply (VccINT)
1.2V	Target Transceiver Power (AVTT)
1.0V	Target Transceiver Power (AVCC)
1.0V	Bridge Transceiver Power (AVTT)
Temp2	microcontroller on-die temperature
Temp2	Board temperature sensor on-die temperature
Temp3	Bridge FPGA on-die temperature
Temp1	Target FPGA on-die temperature

Table 11 : Voltage and Temperature Monitors

An example application that reads the system monitor ("sysmon") is available within the ADM-XRC-KU1 SDK.

3.7.1 Automatic Temperature Monitoring

The onboard system monitor microcontroller contains pre-programmed temperature limits. The temperature limits are shown in Table Temperature Limits:

	Target FPGA		Bridge FPGA		Board	
	Min	Max	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+85 degC	0 degC	+85 degC
Extended	0 degC	+100 degC	0 degC	+100 degC	0 degC	+100 degC
Industrial	-40 degC	+100 degC	-40 degC	+100 degC	-40 degC	+100 degC

Table 12 : Temperature Limits

Important:

If either FPGA temperature limit is exceeded, the Target FPGA is automatically cleared. This is indicated by the Green LED (Target Configured or DONE) switching off and the two status LEDs showing a temperature fault indication. This condition is cleared with a power cycle.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang" as a result of communication errors.

An overtemperature shutdown will not occur until the system monitor reads 5 degC above the maximum limit for multiple samples in a row (i.e. +105 degC for Industrial boards). This is to compensate for potential errors in the temperature readings. There is no protection mechanism in place for minimum temperatures or the "Board" temperature sensor limits.

3.7.2 Microcontroller Status LEDs

LEDs D9 (Red) and D8 (Green) indicate the microcontroller status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 13 : Status LED Definitions

3.8 Local Bus

A Multiplexed Packet Transport Link (MPTL) connects the Bridge and Target FPGAs. It is capable of transferring data at up to 2GB/s simultaneously in each direction.

The MPTL replaces the parallel local bus used in previous generations of the ADM-XRC series. Details of the link and example designs are given in the ADM-XRC-KU1 Software Development Kit (SDK).

3.9 Target FPGA

3.9.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the ADM-XRC-KU1 SDK.

IO Banks	Voltage	Purpose
0, 65	3.3V	Configuration, JTAG, Target SelectMap Interface, QSPI Flash, Pn4 GPIO
44	1.8V	Pn4 GPIO
64	2.5V	Pn6 GPIO, Local Bus Control
24, 25, 45	XRM_VIO	XRM Interface (variable voltage)
46, 47, 48, 66, 67, 68	1.2V	DRAM Banks 0-3

Table 14 : Target FPGA IO Banks

3.9.2 Target MGT Links

There are a total of 26 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

Links	Width	Connection
MPTL(3:0)	4	MPTL link to Bridge FPGA
PCIe(3:0)	4	XMC Connector P5 lanes (3:0) in Bridge Bypass Mode
PCIe(7:4)	4	Direct link to XMC P5 lanes (7:4)
P6(9:0)	10	Direct link to XMC P6 lanes (9:0)
XRM(7:0)	8	Direct link to XRM interface

Table 15 : Target MGT Links

The connections of these links are shown in MGT Links:

For MGT Clocking see Clocks:

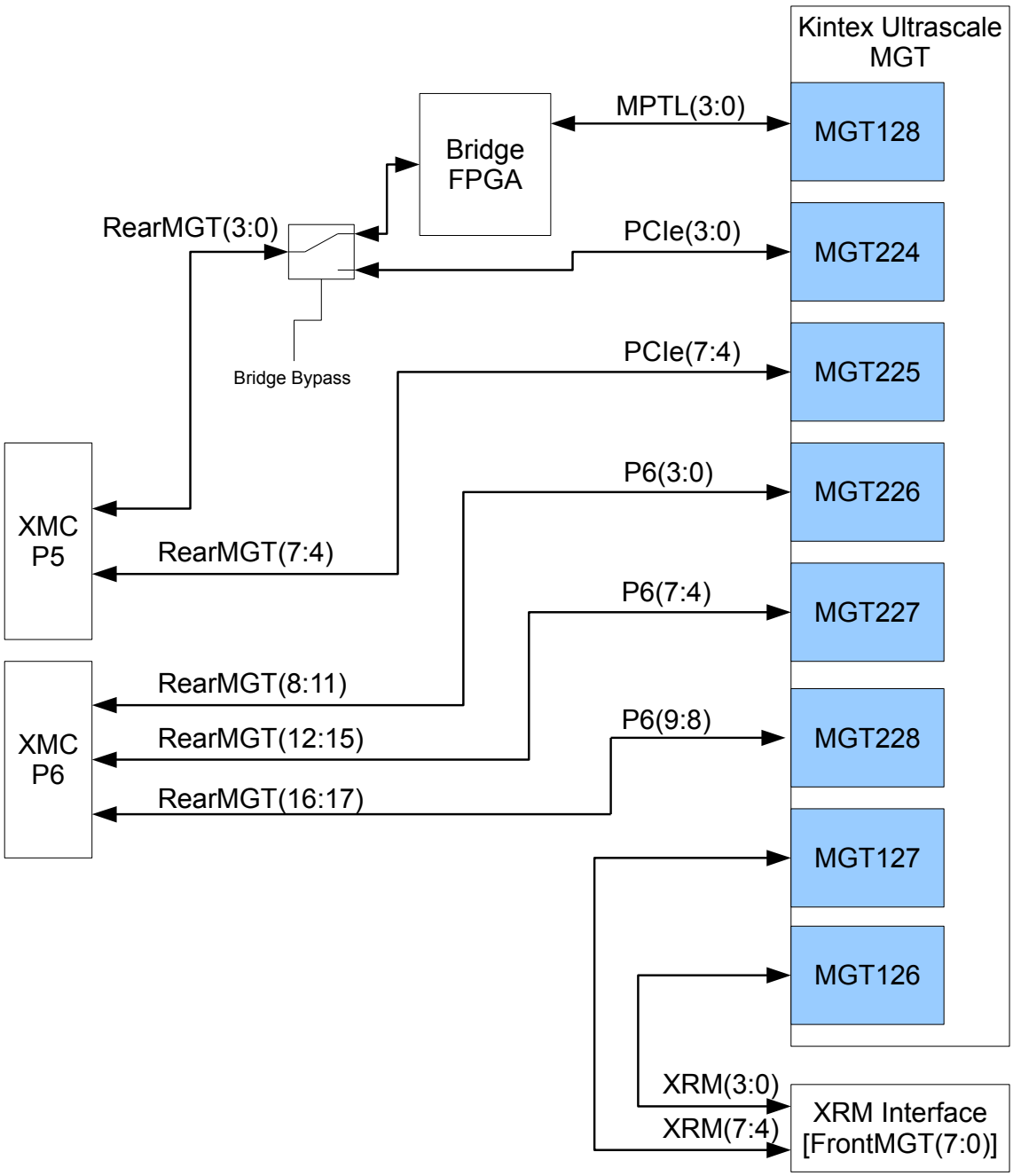


Figure 7 : MGT Links

3.10 Memory Interfaces

The **ADM-XRC-KU1** has four independent banks of DDR4 SDRAM. Each bank consists of two 16 bit wide memory devices in parallel to provide a 32 bit datapath capable of running at up to 1200MHz (DDR-2400). 8Gb devices (Micron MT40A512M16HA-083E) are fitted as standard to provide 2GB per bank.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). DRAM Banks Shows the component references and FPGA banks used. Full details of the interface, signaling standards and an example design are provided in the ADM-XRC-KU1 SDK.

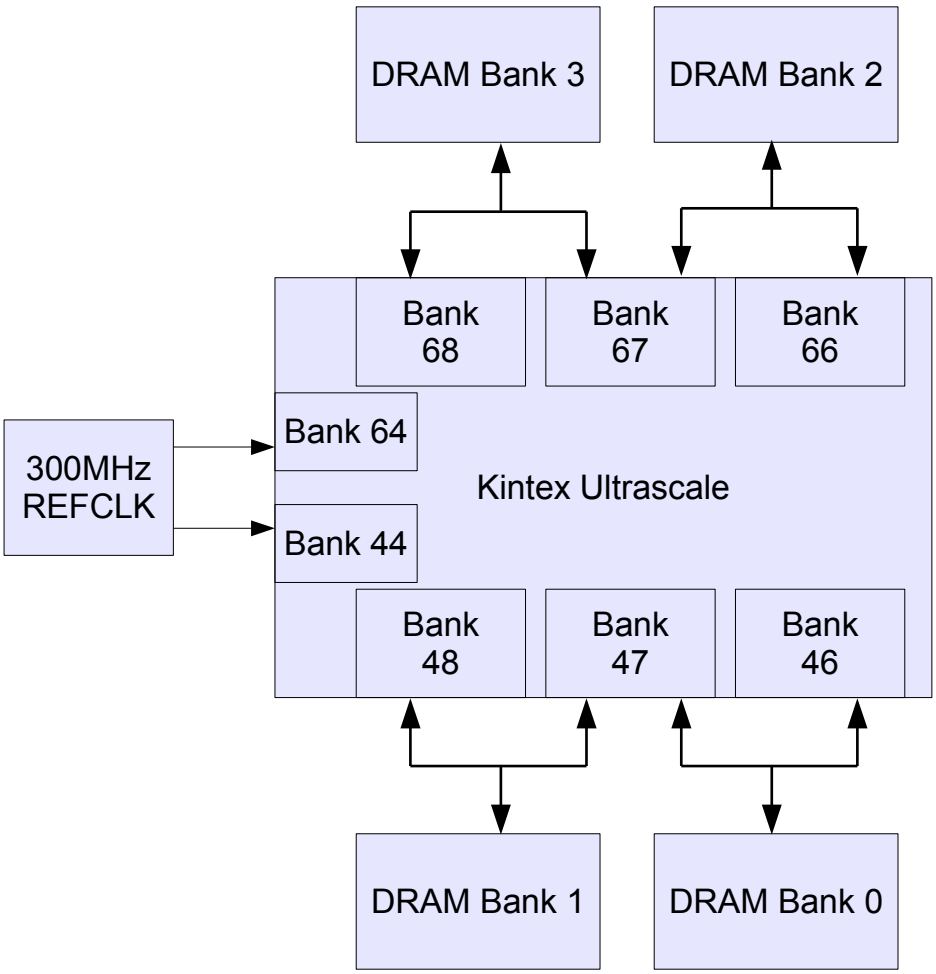


Figure 8 : DRAM Banks

3.11 XRM Interface and Front-Panel I/O

The XRM interface provides a high-performance and flexible front-panel interface through a range of interchangeable XRM modules. Further details of the XRM modules can be found on the Alpha Data website.

The XRM interface consists of two samtec connectors, CN1 and CN2.

3.11.1 XRM Connector, CN1

Connector CN1 is for general purpose signals, power and module control. The connector is a 180-way Samtec connector with 3 fields.

The part fitted to the **ADM-XRC-KU1** is Samtec QSH-090-01-F-D-A-K.

Full pinout information for this connector is listed in XRM Connector CN1, Field 1 to XRM Connector CN1, Field 3.

3.11.2 XRM Connector CN2

Connector CN2 is for the high-speed serial (MGT) links.

The part fitted to the **ADM-XRC-KU1** is Samtec QSE-014-01-F-D-DP-A-K.

Full pinout information for this connector is listed in XRM Connector CN2.

3.11.3 XRM I/F - GPIO

The general purpose IO (GPIO) signals are connected in 4 groups to the Target FPGA. Each group consists of 16 standard I/O pairs, a Regional Clock Capable pair and either 2 or 4 single-ended signals. There are no on-board terminations on the pairs and any can be used in single-ended modes.

To allow fast data transfer, all of the GPIO signals within a group are delay matched to within 100ps.

All the XRM GPIO signals and FPGA IO banks share a common voltage, XRM_VIO, that can be either 1.8V, 1.5V or 1.2V. The required voltage is stored within the platform management PROM on the XRM.

Group	FPGA Bank	Name	Function
Group A	16-17	XRM_DA (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DA_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SA (1:0)	2 single-ended GPIO
Group B	15-16	XRM_DB (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DB_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SB (1:0)	2 single-ended GPIO
Group C	15	XRM_DC (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DC_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SC (1:0)	2 single-ended GPIO
Group D	17	XRM_DD (15:0)	16 diff. Pairs / 32 single-ended
		XRM_DD_CC (16)	Regional Clock / GPIO pair / 2 single-ended
		SD (3:0)	4 single-ended GPIO

Table 16 : XRM GPIO Groups

3.11.4 XRM I/F - High-speed Serial Links

Eight MGT links are routed between the Target FPGA and the XRM interface. Lanes (6:0) are routed through the Samtec QSE-DP connector, CN2. Lane (7) is routed through the Samtec QSH connector, CN1.

3.11.5 XRM IO Voltage Override

Each XRM is built with an I2C EEPROM that contains vital product information (VPD) such as part number, serial number, operating voltage, and product specific information. For designing custom XRMs, contact Alpha-Data for details on duplicating this VPD data.

Alternatively, FORCE2V5_L can be driven low to select 1.8V for the front I/O voltage. Note that FORCE2V5_L is a signal name from a historical design, and the operating voltage will not be 2.5V but rather 1.8V if this mode is used.

3.12 QSPI Flash Memory

A pair of 512Mb QSPI Flash Memory devices (Micron MT25QL512ABB8E12-0AAT) are connected to the Target FPGA on Bank 65 (VCCO=3.3V).

The connections between the QSPI flash devices and the Target FPGA are detailed below:

QSPI Device	Signal Name	FPGA Pin
0	CLK	AN14
0	CS_B	AM14
0	IO[3..0]	AL13 AM15 AL14 AK15
1	CLK	AJ15
1	CS_B	AN12
1	IO[3..0]	AM12 AL12 AJ14 AH14

Table 17 : QSPI Flash Connections

Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

.	A	B	C	D	E	F
1:	PET_P0	PET_N0	3V3	PET_P1	PET_N1	VPWR
2:	GND	GND	-	GND	GND	MRSTI_L
3:	PET_P2	PET_N2	3V3	PET_P3	PET_N3	VPWR
4:	GND	GND	TCK	GND	GND	MRSTO_L
5:	PET_P4	PET_N4	3V3	PET_P5	PET_N5	VPWR
6:	GND	GND	TMS	GND	GND	12V0
7:	PET_P6	PET_N6	3V3	PET_P7	PET_N7	VPWR
8:	GND	GND	TDI	GND	GND	M12V0
9:	-	-	-	-	-	VPWR
10:	GND	GND	TDO	GND	GND	GA0
11:	PER_P0	PER_N0	MBIST_L	PER_P1	PER_N1	VPWR
12:	GND	GND	GA1	GND	GND	MPRESENT_L
13:	PER_P2	PER_N2	3V3_AUX	PER_P3	PER_N3	VPWR
14:	GND	GND	GA2	GND	GND	I2C_SDA
15:	PER_P4	PER_N4	-	PER_P5	PER_N5	VPWR
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	PER_P6	PER_N6	-	PER_P7	PER_N7	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK0_P	REFCLK0_N	-	WAKE_L	ROOT0_L	-

Table 18 : Pn5 Interface

Appendix A.2: Secondary XMC Connector, P6

.	A	B	C	D	E	F
1:	PN6_TX_P0	PN6_TX_N0	X38s_P18	PN6_TX_P1	PN6_TX_N1	X38s_N18
2:	GND	GND	X38s_N16	GND	GND	X38s_N17
3:	PN6_TX_P2	PN6_TX_N2	X38s_P16	PN6_TX_P3	PN6_TX_N3	X38s_P17
4:	GND	GND	X38s_N14	GND	GND	X38s_N15
5:	PN6_TX_P4	PN6_TX_N4	X38s_P14	PN6_TX_P5	PN6_TX_N5	X38s_P15
6:	GND	GND	X38s_N12	GND	GND	X38s_N13
7:	PN6_TX_P6	PN6_TX_N6	X38s_P12	PN6_TX_P7	PN6_TX_N7	X38s_P13
8:	GND	GND	X38s_N10	GND	GND	X38s_N11
9:	PN6_TX_P8	PN6_TX_N8	X38s_P10	PN6_TX_P9	PN6_TX_N9	X38s_P11
10:	GND	GND	X38s_N8	GND	GND	X38s_N9
11:	PN6_RX_P0	PN6_RX_N0	X38s_P8	PN6_RX_P1	PN6_RX_N1	X38s_P9
12:	GND	GND	X38s_N6	GND	GND	X38s_N7
13:	PN6_RX_P2	PN6_RX_N2	X38s_P6	PN6_RX_P3	PN6_RX_N3	X38s_P7
14:	GND	GND	X38s_N4	GND	GND	X38s_N5
15:	PN6_RX_P4	PN6_RX_N4	X38s_P4	PN6_RX_P5	PN6_RX_N5	X38s_P5
16:	GND	GND	X38s_N2	GND	GND	X38s_N3
17:	PN6_RX_P6	PN6_RX_N6	X38s_P2	PN6_RX_P7	PN6_RX_N7	X38s_P3
18:	GND	GND	X38s_N0	GND	GND	X38s_N1
19:	PN6_REFCLK_P*	PN6_REFCLK_N*	X38s_P0	PN6_RX_P9	PN6_RX_N9	X38s_P1

Table 19 : Pn6 Interface

*** = Determined via the IO ordering option:**

- Default (blank) = Pair designated as an external clock input (PN6_REFCLK_P & PN6_REFCLK_N).
- /10RX = External Clock input replaced by data input (PN6_RX_P8 & PN6_RX_N8).

Appendix A.2.1: Pn6 GPIO Pin Map

Signal	FPGA Pin	FPGA Bank
X38s_P0	AT19	64
X38s_N0	AU19	64
X38s_P1	AR20	64
X38s_N1	AT20	64
X38s_P2	AT18	64
X38s_N2	AT17	64
X38s_P3	AV19	64
X38s_N3	AW18	64
X38s_P4	AR18	64
X38s_N4	AR17	64
X38s_P5	AU17	64
X38s_N5	AU16	64
X38s_P6	AP19	64
X38s_N6	AP18	64
X38s_P7	AP16	64
X38s_N7	AR16	64
X38s_P8	AK18	64
X38s_N8	AK17	64
X38s_P9	AL19	64
X38s_N9	AL18	64
X38s_P10	AH17	64
X38s_N10	AH16	64
X38s_P11	AJ19	64
X38s_N11	AJ18	64
X38s_P12	AH19	64
X38s_N12	AH18	64
X38s_P13	AJ16	64
X38s_N13	AK16	64
X38s_P14	AE17	64
X38s_N14	AF17	64
X38s_P15	AG17	64
X38s_N15	AG16	64
X38s_P16	AE18	64
X38s_N16	AF18	64
X38s_P17	AD16	64

Table 20 : Pn6 GPIO Pin Map (continued on next page)

Signal	FPGA Pin	FPGA Bank
X38s_N17	AE16	64
X38s_P18	AF19	64
X38s_N18	AG19	64

Table 20 : Pn6 GPIO Pin Map

Appendix A.3: PMC Connector P4

Signal	FPGA Pin	Clock Capability	P4 Pin	P4 Pin	Clock Capability	FPGA Pin	Signal
PN4_P1	AG21	DBC	1	2	-	AV23	PN4_P2
PN4_N1	AG22	DBC	3	4	-	AW23	PN4_N2
PN4_P3	AN24	QBC	5	6	-	AT23	PN4_P4
PN4_N3	AP24	QBC	7	8	-	AT24	PN4_N4
PN4_P5	AM22	GC	9	10	-	AN23	PN4_P6
PN4_N5	AN22	GC	11	12	-	AP23	PN4_N6
PN4_P7	AK20	-	13	14	-	AE23	PN4_P8
PN4_N7	AK21	-	15	16	-	AF23	PN4_N8
PN4_P9	AE22	-	17	18	-	AD20	PN4_P10
PN4_N9	AF22	-	19	20	-	AD21	PN4_N10
PN4_P11	AL20	-	21	22	DBC	AE20	PN4_P12
PN4_N11	AM20	-	23	24	DBC	AE21	PN4_N12
PN4_P13	AK23	GC + QBC	25	26	-	AH22	PN4_P14
PN4_N13	AL23	GC + QBC	27	28	-	AH23	PN4_N14
PN4_P15	AP21	QBC	29	30	-	AF20	PN4_P16
PN4_N15	AR21	QBC	31	32	-	AG20	PN4_N16
PN4_P17	AV24	DBC	33	34	QBC	AJ20	PN4_P18
PN4_N17	AW24	DBC	35	36	QBC	AJ21	PN4_N18
PN4_P19	AU21	DBC	37	38	-	AR22	PN4_P20
PN4_N19	AV22	DBC	39	40	-	AR23	PN4_N20
PN4_P21	AT22	-	41	42	-	AV21	PN4_P22
PN4_N21	AU22	-	43	44	-	AW21	PN4_N22
PN4_P23	AP20*	-	45	46	-	AU24*	PN4_P24
PN4_N23	AJ23*	-	47	48	-	AH21*	PN4_N24
PN4_P25	AR13	QBC	49	50	-	AP15	PN4_P26
PN4_N25	AT13	QBC	51	52	-	AR15	PN4_N26
PN4_P27	AT14	-	53	54	DBC	AT15	PN4_P28
PN4_N27	AU14	-	55	56	DBC	AU15	PN4_N28
PN4_P29	AU12	-	57	58	-	AV13	PN4_P30
PN4_N29	AV12	-	59	60	-	AW13	PN4_N30
PN4_P31	AV14	-	61	62	-	AV16	PN4_P32
PN4_N31	AW14	-	63	64	-	AW16	PN4_N32

Table 21 : Pn4 Interface

Table Notes:

- GC: Global clock QBC: Quad byte clock DBC: Dedicated byte clock
- ***** : Single ended signal only, cannot be used as part of a differential pair.
- ****** : Single ended signal only (LVCMOS / LVTTL). Signal on HD Bank 65 with VCCO = 3.3V, hence cannot

be used as part of a differential pair.

Appendix A.4: Rear MGT Connections to the Target FPGA

In normal mode, the target FPGA RearMGT lanes (3:0) are connected to the Bridge FPGA. In Bridge Bypass Mode, they are connected to P5 lanes (3:0).

RearMGT Lanes (7:4) are connected directly to P5 lanes (7:4).

RearMGT Lanes (17:8) are connected directly to P6 lanes (9:0).

The pin mappings are as follows:

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
RearMGT_TX_0	AW8	AW7	P5.A1	P5.B1
RearMGT_TX_1	AV6	AV5	P5.D1	P5.E1
RearMGT_TX_2	AU8	AU7	P5.A3	P5.B3
RearMGT_TX_3	AT6	AT5	P5.D3	P5.E3
RearMGT_TX_4	AR8	AR7	P5.A5	P5.B5
RearMGT_TX_5	AP6	AP5	P5.D5	P5.E5
RearMGT_TX_6	AN8	AN7	P5.A7	P5.B7
RearMGT_TX_7	AM6	AM5	P5.D7	P5.E7
RearMGT_TX_8	AL8	AL7	P6.A1	P6.B1
RearMGT_TX_9	AK6	AK5	P6.D1	P6.E1
RearMGT_TX_10	AJ8	AJ7	P6.A3	P6.B3
RearMGT_TX_11	AH6	AH5	P6.D3	P6.E3
RearMGT_TX_12	AG8	AG7	P6.A5	P6.B5
RearMGT_TX_13	AF6	AF5	P6.D5	P6.E5
RearMGT_TX_14	AE4	AE3	P6.A7	P6.B7
RearMGT_TX_15	AD6	AD5	P6.D7	P6.E7
RearMGT_TX_16	AB6	AB5	P6.A9	P6.B9
RearMGT_TX_17	AA4	AA3	P6.D9	P6.E9
-	-	-	-	-
RearMGT_RX_0	AW4	AW3	P5.A11	P5.B11
RearMGT_RX_1	AV2	AV1	P5.D11	P5.E11
RearMGT_RX_2	AU4	AU3	P5.A13	P5.B13
RearMGT_RX_3	AT2	AT1	P5.D13	P5.E13
RearMGT_RX_4	AR4	AR3	P5.A15	P5.B15
RearMGT_RX_5	AP2	AP1	P5.D15	P5.E15
RearMGT_RX_6	AN4	AN3	P5.A17	P5.B17
RearMGT_RX_7	AM2	AM1	P5.D17	P5.E17
RearMGT_RX_8	AL4	AL3	P6.A11	P6.B11
RearMGT_RX_9	AK2	AK1	P6.D11	P6.E11
RearMGT_RX_10	AJ4	AJ3	P6.A13	P6.B13

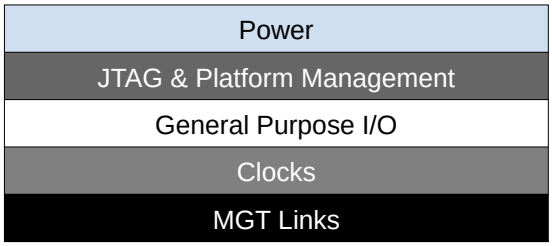
Table 22 : Target RearMGT Mapping (continued on next page)

Signal	FPGA + Pin	FPGA - Pin	Rear Connector + Pin	Rear Connector - Pin
RearMGT_RX_11	AH2	AH1	P6.D13	P6.E13
RearMGT_RX_12	AG4	AG3	P6.A15	P6.B15
RearMGT_RX_13	AF2	AF1	P6.D15	P6.E15
RearMGT_RX_14	AD2	AD1	P6.A17	P6.B17
RearMGT_RX_15	AC4	AC3	P6.D17	P6.E17
RearMGT_RX_16	AB2	AB1	P6.A19	P6.B19
RearMGT_RX_17	Y2	Y1	P6.D19	P6.E19

Table 22 : Target RearMGT Mapping

Appendix B: Front (XRM) Connector Pinouts

The XRM interface consists of two connectors: CN1 and CN2. CN1 is a 180-way Samtec QSH in 3 fields. It is for general purpose signals, power and module control. CN2 is a 28-way Samtec QSE-DP for high-speed serial (MGT) links.



Appendix B.1: XRM Connector CN1, Field 1

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DA_N0	AW31	1	2	AW29	DA_N1
DA_P0	AW30	3	4	AV29	DA_P1
DA_N2	AV32	5	6	AN33	DA_P3
DA_P2	AU32	7	8	AP33	DA_N3
DA_N4	AV31	9	10	AP31	DA_N5
DA_P4	AU31	11	12	AP30	DA_P5
DA_N6	AR32	13	14	AK33	DA_N7
DA_P6	AR31	15	16	AJ33	DA_P7
DA_P8	AT29	17	18	AL30	DA_P9
DA_N8	AT30	19	20	AM30	DA_N9
DA_N10	AR30	21	22	AK31	DA_N11
DA_P10	AP29	23	24	AJ31	DA_P11
DA_N12	AU30	25	26	AJ30	DA_P13
DA_P12	AU29	27	28	AK30	DA_N13
DA_N14	AM29	29	30	AK32	DA_P15
DA_P14	AL29	31	32	AL32	DA_N15
DB_N0	AF28	33	34	AV39	DB_N1
DB_P0	AE28	35	36	AV38	DB_P1
SA_0	AN29	37	38	AM32	DA_CC_P16
3V3	-	39	40	AN32	DA_CC_N16
3V3	-	41	42	-	FORCE2V5_L
3V3	-	43	44	-	2V5
5V0	-	45	46	-	VREF
5V0	-	47	48	-	VccIO
VBATT	-	49	50	-	VccIO
12V0	-	51	52	-	VccIO
12V0	-	53	54	-	M12V0
PRESENCE_L	-	55	56	-	TDI
TCK	-	57	58	-	TRST
TMS	-	59	60	-	TDO

Table 23 : XRM Connector CN1, Field 1

Appendix B.2: XRM Connector CN1, Field 2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DB_N2	AU34	61	62	AJ29	DB_N3
DB_P2	AT34	63	64	AH29	DB_P3
DB_N4	AU35	65	66	AW36	DB_N5
DB_P4	AT35	67	68	AW35	DB_P5
DB_N6	AH32	69	70	AG29	DB_N7
DB_P6	AH31	71	72	AF29	DB_P7
DB_N8	AV36	73	74	AV33	DB_P9
DB_P8	AU36	75	76	AV34	DB_N9
DB_P10	AH28	77	78	AF30	DB_N11
DB_N10	AJ28	79	80	AE30	DB_P11
DB_N12	AU39	81	82	AU37	DB_P13
DB_P12	AT39	83	84	AV37	DB_N13
DB_N14	AT33	85	86	AW34	DB_N15
DB_P14	AR33	87	88	AW33	DB_P15
DB_CC_P16	AR37	89	90	AW38	SB_1
DB_CC_N16	AT37	91	92	AK26	SC_0
SA_1	AL33	93	94	AH27	SC_1
SB_0	AG30	95	96	AV27	SD_0
DC_CC_P16	AM26	97	98	AG24	DC_N1
DC_CC_N16	AN26	99	100	AF24	DC_P1
DC_N0	AJ24	101	102	AM27	DD_CC_P16
DC_P0	AH24	103	104	AN27	DD_CC_N16
SD_1	AJ39	105	106	AV26	SD_3
SD_2	AP35	107	108	AT38	GCLK_M2C_N
MGTCLK_M2C_P	AD32	109	110	AR38	GCLK_M2C_P
MGTCLK_M2C_N	AD33	111	112	-	SDA
XRM_LVDS_C-LK_N	AN31	113	114	-	SCL
XRM_LVDS_C-LK_P	AM31	115	116	-	ALERT_N
MGT_C2M_P7	W34	117	118	V36	MGT_M2C_P7
MGT_C2M_N7	W35	119	120	V37	MGT_M2C_N7

Table 24 : XRM Connector CN1, Field 2

Appendix B.3: XRM Connector CN1, Field 3

Signal	FPGA	Samtec	Samtec	FPGA	Signal
DC_P2	AD26	121	122	AR26	DC_P3
DC_N2	AE26	123	124	AR27	DC_N3
DC_N4	AF27	125	126	AD25	DC_P5
DC_P4	AE27	127	128	AE25	DC_N5
DC_P6	AF25	129	130	AL24	DC_P7
DC_N6	AG25	131	132	AL25	DC_N7
DC_N8	AG27	133	134	AK25	DC_N9
DC_P8	AG26	135	136	AJ25	DC_P9
DC_P10	AH26	137	138	AM25	DC_N11
DC_N10	AJ26	139	140	AM24	DC_P11
DC_P12	AL27	141	142	AP28	DC_N13
DC_N12	AL28	143	144	AN28	DC_P13
DC_N14	AK28	145	146	AK35	DD_P1
DC_P14	AK27	147	148	AK36	DD_N1
DD_P0	AL39	149	150	AR25	DC_N15
DD_N0	AM39	151	152	AP25	DC_P15
DD_P2	AM36	153	154	AK38	DD_N3
DD_N2	AM37	155	156	AK37	DD_P3
DD_N4	AP39	157	158	AL38	DD_N5
DD_P4	AN39	159	160	AL37	DD_P5
DD_P6	AN38	161	162	AU26	DD_N7
DD_N6	AP38	163	164	AU25	DD_P7
DD_N8	AR36	165	166	AL35	DD_N9
DD_P8	AP36	167	168	AL34	DD_P9
DD_N10	AM35	169	170	AW28	DD_N11
DD_P10	AM34	171	172	AV28	DD_P11
DD_N12	AP34	173	174	AU27	DD_N13
DD_P12	AN34	175	176	AT27	DD_P13
DD_N14	AN37	177	178	AW26	DD_N15
DD_P14	AN36	179	180	AW25	DD_P15

Table 25 : XRM Connector CN1, Field 3

Appendix B.4: XRM Connector CN2

Signal	FPGA	Samtec	Samtec	FPGA	Signal
MGT_C2M_P0	AH36	1	2	AG38	MGT_M2C_P0
MGT_C2M_N0	AH37	3	4	AG39	MGT_M2C_N0
MGT_C2M_P1	AG34	5	6	AF36	MGT_M2C_P1
MGT_C2M_N1	AG35	7	8	AF37	MGT_M2C_N1
MGT_C2M_P4	AC34	9	10	AB36	MGT_M2C_P4
MGT_C2M_N4	AC35	11	12	AB37	MGT_M2C_N4
MGT_C2M_P5	AA34	13	14	AA38	MGT_M2C_P5
MGT_C2M_N5	AA35	15	16	AA39	MGT_M2C_N5
MGT_C2M_P2	AE34	17	18	AE38	MGT_M2C_P2
MGT_C2M_N2	AE35	19	20	AE39	MGT_M2C_N2
MGT_C2M_P3	AD36	21	22	AC38	MGT_M2C_P3
MGT_C2M_N3	AD37	23	24	AC39	MGT_M2C_N3
MGT_C2M_P6	Y36	25	26	W38	MGT_M2C_P6
MGT_C2M_N6	Y37	27	28	W39	MGT_M2C_N6

Table 26 : XRM Connector CN2

Revision History

Date	Revision	Nature of Change
26 Oct 2015	0.1	Initial Draft
29 Jan 2016	0.2	Still Draft - fixed errors in XRM table and Flash table
08 Feb 2016	0.3	Still Draft - updated after feedback comments
18 Feb 2016	1.0	First Release
19 Feb 2016	1.1	Amended block diagram and Pn6 table
09 May 2016	1.2	Amended Flash Memory Map
17 Aug 2016	1.3	Added note regarding bridge bypass LED
22 Nov 2016	1.4	Fixed error in table 14 (bank 64 voltage was incorrect)
09 Feb 2017	1.5	Fixed error in table 3 (LED D7 description was incorrect)
14 Jun 2017	1.6	Fixed error in Section 3.2.3 (MVMRO LED number was incorrect)
10 Nov 2017	1.7	Fixed error in Section 3.7.2 (Status LED table was incomplete)
22 Mar 2018	1.8	Fixed error in Table 14 (bank 44+65 descriptions were incorrect)
09 May 2019	1.9	Added details on QSPI Flash
05 Feb 2020	1.10	Added footnote to Table 21 regarding Pn4 GPIO
12 May 2020	1.11	Minor change to section 3.5 (Flash Memory)
11 Jun 2020	1.12	Changes to section 3.7.1 (Temperature monitoring)
08 Jun 2023	1.13	Removed dead link to heatsink environmental specifications

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